REV LTR	DESCRIPTION	DATE	APPVD.
-	Orig. Release	02/15/08	JSN
A	Revised per ECN 2012-1	11/09/12	JSN
B	Revised per ECN 2014-1	03/26/14	JSN
C	Revised per ECN 2016-2	10/21/16	JSN

FTTC11 Series

CMOS/LVDS/LVEPCL/CML Output TCXO/VCTCXO

FOR SPACE APPLICATIONS

10MHz to 1400MHz

(5 x 7 mm, SMD, 1.8V, 2.5 V,3.3V)

(Refer to Page 5 for Models with Reduced Screening & QCI)

6.0 Part Numbering Example:

FTTC11 – L S 3 J D T 100

L – Output logic
H=CMOS
L=LVDS
P=LVPECL
M=CML

S – Grade(Screening Level)
N=No Screening
I= Industrial Std
B= MIL-PRF-55310,level B
S= MIL-PRF-55310,level S ,50krad(Si) total dose
V= MIL-PRF-55310,level S ,80krad(Si) total dose
R= MIL-PRF-55310,level S ,100krad(Si) total dose

3 – Voltage
3=+3.3V
2=+2.5V
1=+1.8V

J – * Frequency stability
G= 1.0 ppm
J = 2.0ppm
K= 6.0ppm
H= 8.0 ppm
L = 9.2ppm
E = 10 ppm

D – Operating temperature range
A= 0°C to +50°C
B= 0°C to +70°C
C= -20°C to +70°C
D= -40°C to +85°C
E= -55°C to +105°C
F= -55°C to +125 °C

T – Frequency tuning
T=TCXO(No Vc)
V=TCVCXO(With Vc)

100 – Frequency MHz

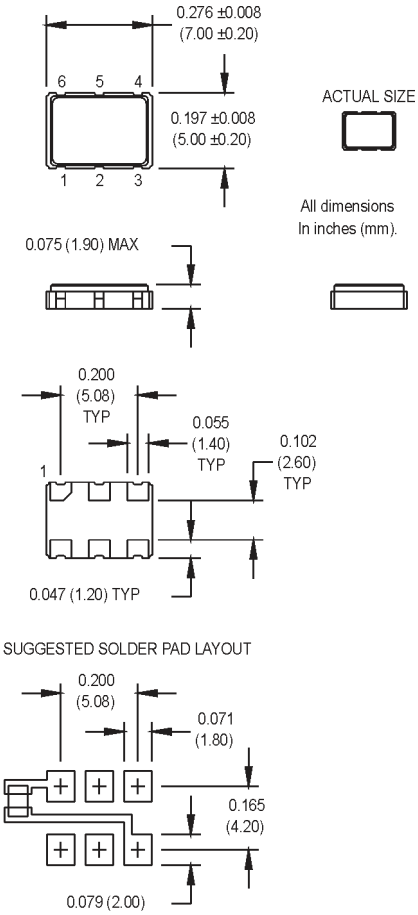
*Note: Frequency stability=(Fmax-Fmin)/2

Freq. Vs Temp Availability

Temp (°C)	G: ±1.0ppm	J: ±2.0ppm	K: ±6.0ppm	H: ±8.0ppm	L: ±9.2ppm
A: 0°C to +50°C	♦	♦	♦	♦	♦
B: 0°C to +70°C	♦	♦	♦	♦	♦
C: -20°C to +70°C	o	♦	♦	♦	♦
D: -40°C to +85°C	o	♦	♦	♦	♦
E: -55°C to +105°C	o	o	o	♦	♦
F: -55°C to +125°C	o	o	o	o	♦

o Contact Factory
♦ available

Product Dimension:



Pin connections:

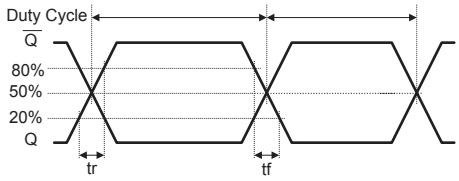
LVPECL, LVDS,CML

Pin #	Connection
1	N/C or Vc
2	N/C
3	GND
4	Output
5	$\overline{\text{Output}}$
6	Supply Voltage

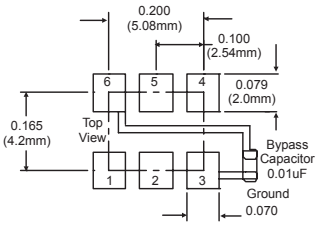
CMOS

Pin #	Connection
1	N/C or Vc
2	N/C
3	GND
4	Output
5*	N/C
6	Supply Voltage

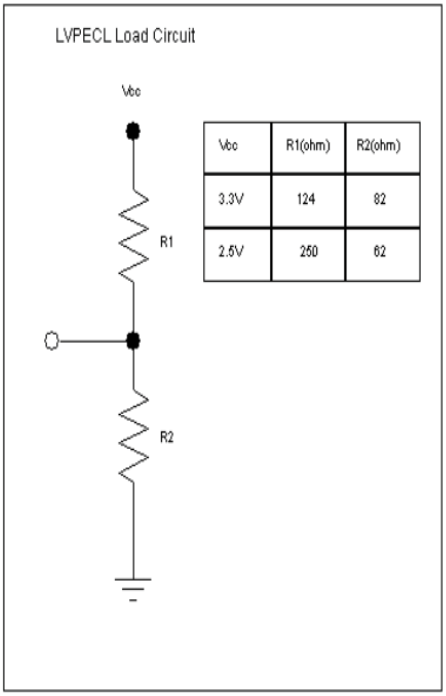
Output Waveform

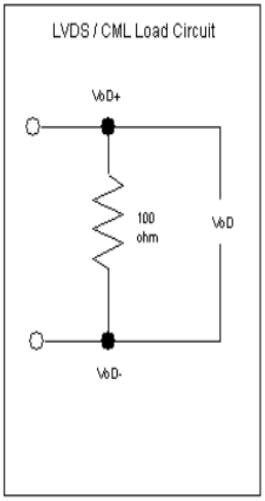


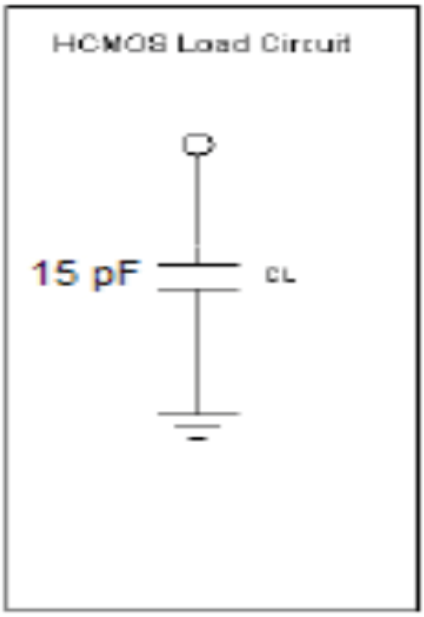
Suggested Pad Layout



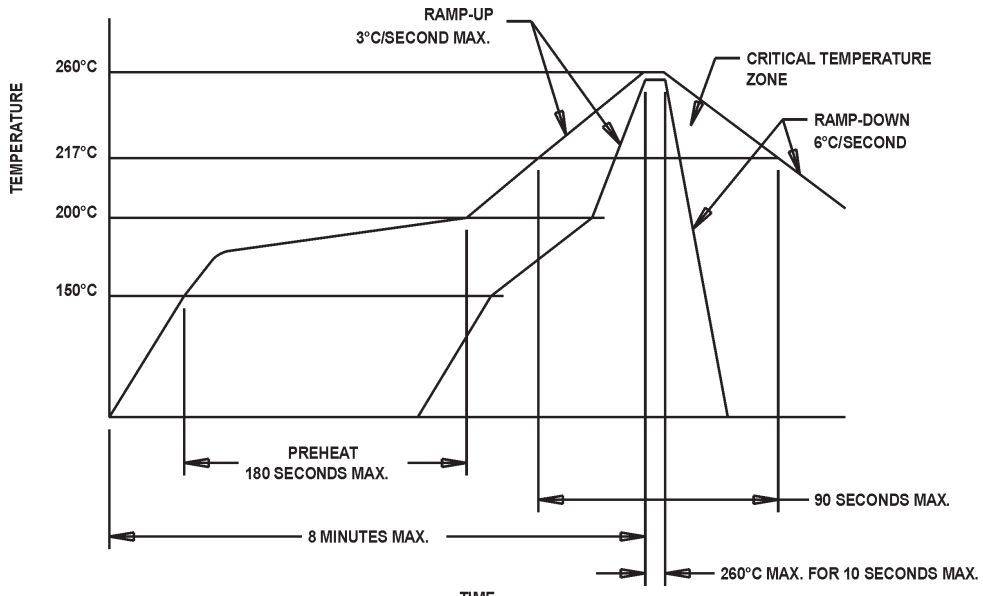
Typical Test Circuit & Load Circuit Diagrams







Maximum Soldering Conditions



	Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions/Notes
Electrical Specifications	Frequency Range		F	10 10		1400 200	MHz MHz	LVPECL, LVDS, CML CMOS
	Operating Temperature		T_A	See How to order			℃	
	Storage Temperature		T_{STG}	-55		+125	℃	
	Frequency Stability			See how to order			ppm	
	Frequency Tolerance at +25℃			-5.0		+5.0	ppm	at time of shiopment
	Frequency Vs. Aging			-2.0 -1.0		+ 2.0 + 1.0	ppm ppm	1st year Thereafter(per year).
	Frequency Vs. Supply Voltage				± 0.5		ppm	5% voltage variation
	Frequency Vs. Reflow				± 0.80		ppm	2 reflows max.
	Frequency Vs. Load				± 0.5		ppm	5% supply voltage variation
	Operating Voltage		$V_{cc}/V_s/V_{dd}$	3.135 2.375 1.71	3.3 2.5 1.8	3.465 2.625 1.89	V V V	
	Operating Current		I_{CC}			130 110 120 100	mA mA mA mA	LVPECL LVDS CML CMOS
	Rise/Fall Time		Tr/Tf			1.0 8	ns ns	PECL, LVPECL, LVDS CMOS
	Logic "1" Level		V_{OH}	V_{CC}-1.02 80% V_{dd}			V V	LVPECL CMOS
	Logic "0" Level		V_{OL}			V_{CC}-1.63 20% V_{dd}	V V	LVPECL CMOS
	Common Mode Output Voltage		Vcm		1.2		V	LVDS
	Symmetry (Duty Cycle)			40 40 40		60 60 60	% % %	@ 50% Vdd (CMOS) @ 50% of waveform (LVPECL) @ 1.25 V (LVDS)
	Output Voltage Level			0.7	0.95	1.2	Vp-p	CML
	Tuning Range			± 5			ppm	VCTCXO only. See Note 2.
	Output Skew				20 15 20		ps ps ps	LVPECL CML LVDS
	Output Load			50 ohm to (V_{CC}-2V) VDC 100 ohm Differential 15			 pF	See Note 3 LVPECL LVDS, CML CMOS
	Enable/Disable Function			80% 80%		0.5 0.5	 V V 	Outputs enabled Outputs disabled Outputs enabled Outputs disabled
	Phase Noise (Typical)		10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	Offset from carrier
	@ 622.080 MHz (LVPECL) @ 100.000 MHz (HCMOS) @ 50.000 MHZ (HCMOS)		-60 -73 -80	-90 -97 -102	-120 -123 -130	-127 -131 -137	-133 -136 -141	dBc/Hz dBc/Hz dBc/Hz
	Jitter	Phase jitter	0.5ps (Typical)@Integrated,Bandwidth 12KHz to 20MHz ,RMS					
		Random period jitter	3.0ps (Typical)@Integrated,Bandwidth 10KHz to 1MHz ,RMS					
		Pk to Pk jitter	20.0ps (Typical)					
Environmental	Shock		Per MIL-STD-202, Method 213, Condition C					
	Vibration		Per MIL-STD-202, Methods 201 & 204					
	Solderability		Per EIAJ-STD-002					
	Hermeticity		1 X 10^{-8} atm cc/sec of helium (Crystal only)					
	Thermal Shock		Per MIL-STD-883, Method 1011, Condition A					
	Thermal Cycle		Per MIL-STD-883, Method 1010, Condition B					

Note 1: Standard ±5ppm(Max),other frequency tolerance,pls factory
Note 2: Contact factory for other Tuning Range options.
Note 3: See Load Circuit Diagram.