FTX2 Series High Reliability 5x7mm Ceramic LVDS/LVPECL Clock Oscillator

Product Features

- High speed-Ultra Low Jitter LVDS , LVPECL , CMLoutput
- 0.75MHz to 1500 MHz Frequency Range
- 1.8V /2.5V /3.3V/ logic levels
- Wide operating temperature range
- Military and space screening tests avaliable
- Calculated MTBF is 3.8×10^6 hours at 125℃

Applications

- FPGA/ASIC Clock Generations
- Military and Space Applications
- Extended temperature applications
- Avionics Flight Controls
- Test and Measurement Equipments
- Clock and Data Recovery

HOW TO ORDER

FTX2 – L W E B / 200

L — Voltage
R=+1.8V
N=+2.5V
L=+3.3V

W — Output Logic
W = LVDS
P = LVPECL
M = CML
C = CMOS

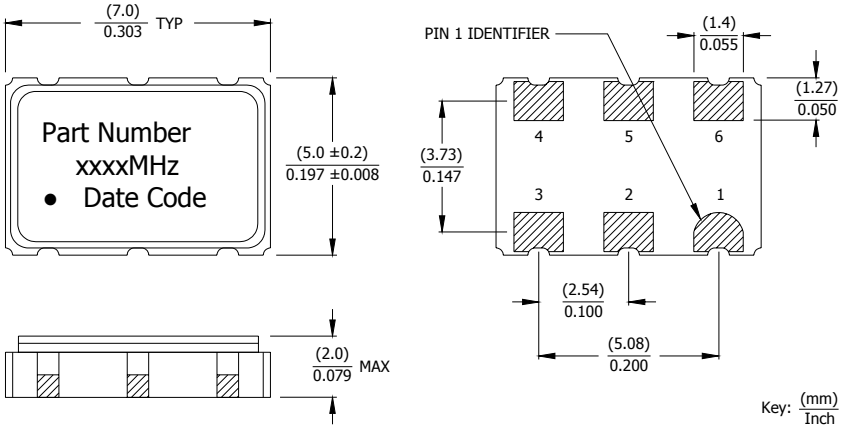
E — Frequency/ Temperature Stability
A = 100 ppm over -40°C to +85°C
B = 50 ppm over -40°C to +85°C
C = 25 ppm over -40°C to +85°C
D = 100 ppm over -55°C to +125°C
E = 50 ppm over -55°C to +125°C
F = 10 ppm over -55°C to +125 °C

B — Screening Level
N = No Screening
I = Industrial Std
B = MIL-PRF-55310D ,level B
S = MIL-PRF-55310D ,level S
V = MIL-PRF-55310D ,level S 100krad(Si) total dose

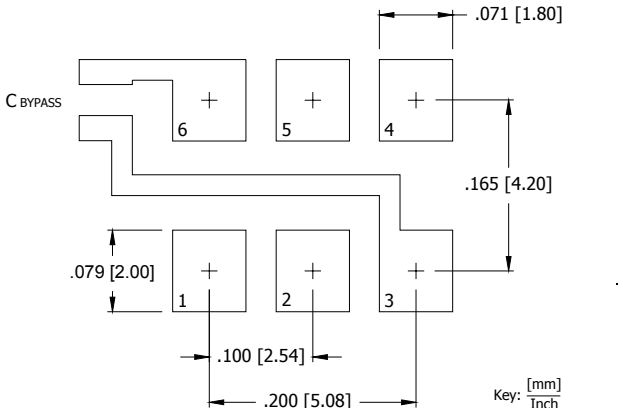
200 — Frequency(MHz)

Package &Size

PACKAGE DRAWING



SUGGESTED SOLDER PAD LAYOUT



Pin Connections

PIN	SYMBOL	DESCRIPTION
1	N/C or EOH	No Connect or Enable
2	N/C or EOH	No Connect or Enable
3	GND	Circuit & Package Ground
4	Output	RF Output
5	Output	Complimentary RF Output
6	V_{CC}	Supply Voltage

FTX2 Series High Reliability 5x7mm Ceramic LVDS/LVPECL Clock Oscillator

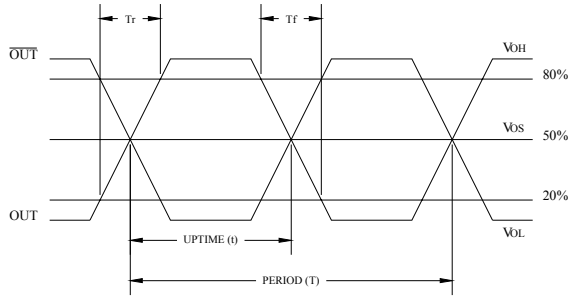
Electrical Performance

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Absolute Maximums	Maximum Supply Voltage	V_{CC}	-	-0.5	-	5.0	V
	Storage Temperature	T_{STG}	-	-55	-	125	°C
	Frequency Range LVPECL and LVDS	f_O	-	0.75		1500	MHz
	Frequency Stability	$\Delta f/f_O$	-	-	-	20, 25, 50 or 100	± ppm
	Operating Temperature Commercial Industrial Military	T_A	-	 -20 -40 -55	25	 70 85 125	°C
Electrical and Waveform Parameters	Supply Voltage(Optional 1.8V)	V_{CC}	± 5 %	2.38 3.14	2.5 3.3	2.63 3.47	V
	Supply Current LVPECL LVDS	I_{CC}	Maximum Load	 - -	 50 25	 120 100	mA
	Start Up Time	T_S	Application of V_{CC}	-	3	5	ms
	Phase Jitter	tjrms	Bandwidth 12 kHz - 20 MHz	-	-	1	ps RMS
	Period Jitter	pjrms	-	-	-	5	ps RMS
	Enable Function Enable Input Voltage Disable Input Voltage	 V_{IH} V_{IL}	Standby Pin 1 or Pin 2 Logic '1', Output Enabled Pin 1 or Pin 2 Logic '0', Output Disabled	 0.7*V_{CC} -	 - -	 - 0.3*V_{CC}	V
	Disable Current	I_{IL}	Pin 1 or Pin 2 Logic '1', Output Disabled	-	-	20	uA
	Enable Time	T_{PLZ}	Pin 1 or Pin 2 Logic '1'	-	-	5	ns
	LVPECL WAVEFORM						
	Output Load	R_L	-	-	50	-	Ohms
	Output Duty Cycle	SYM	@ V_{CC} - 1.3V	45	-	55	%
	Output Voltage Levels Logic '1' Level Logic '0' Level	 V_{OH} V_{OL}	 PECL Load PECL Load	 V_{CC} - 1.025V -	 - -	 - V_{CC} - 1.62V	V
	Rise and Fall Time f_O < 100 MHz f_O > 100 MHz	 T_R, T_F	 @ 20% - 80% Levels	 - -	 0.8 0.5	 2.5 2.0	ns
	LVDS WAVEFORM						
	Output Load	R_L	Between Outputs	-	100	-	Ohms
	Output Duty Cycle	SYM	@ 1.25V	45	-	55	%
	Differential Output Voltage	V_{OD}	RL = 100 Ohms	247	350	454	mV
	Differential Output Error	-	-	-	-	50	mV
	Offset Voltage	V_{OS}	LVDS Load	1.125	1.25	1.375	V
	Offset Error	-	-	-	-	50	mV
	Output Voltage Levels Logic '1' Level Logic '0' Level	 V_{OH} V_{OL}	 LVDS Load LVDS Load	 - 0.8	 1.43 1.1	 1.7 -	V
	Rise and Fall Time f_O < 100 MHz f_O > 100 MHz	 T_R, T_F	 @ 20% - 80% Levels	 - -	 0.8 0.5	 2.5 2.0	ns

Notes:

1. Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 10 year aging.

PECL/LVDS OUTPUT WAVEFORM



DUTY CYCLE = t/T x 100 (%)

ENABLE TRUTH TABLE

PIN 1 or PIN 2	PIN 4 / PIN 5
Logic '1'	Output
Open	Output
Logic '0'	High Imp.