

FTX4 Series High Reliability 3.2 x 2.5mm Ceramic CMOS/TTL Clock Oscillator

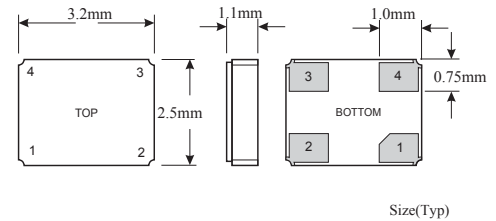
Product Features

- <1 ps RMS Ultra Low Jitter
- 1MHz to 160 MHz (32.786KHz available)
- 1.8V /2.5V/3.3V/5.0V logic levels
- Hermetically sealed ceramic packages
- Wide operating temperature range
- Military and space screening tests available
- High shock resistance(meet 35000G shock)
- Pb-free and RoHS/Green compliant

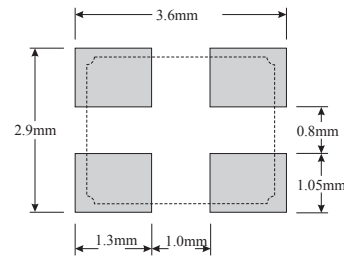
Applications

- High shock and vibration environments
- Military and space applications
- Extended temperature applications
- Down-hole drilling Equipments
- Instrumentation and Microprocessor

DIMENSIONS



SUGGESTED LANDPATTERN



PIN CONNECTIONS

1. Not connected (N) or Enable/Disable (E)
2. Ground
3. Output
4. V_{DD}

HOW TO ORDER

FTX4

-

E

L

B

N /

100

Frequency/Temperature Stability
 A= 100 ppm over -40°C to +85°C
 B= 50 ppm over -40°C to +85°C
 C= 25 ppm over -40°C to +85°C
 D= 100 ppm over -55°C to +125°C
 E= 50 ppm over -55°C to +125°C
 F= 20 ppm over -20°C to +70 °C
 G= 50 ppm over -20°C to +70 °C

Voltage
 R=+1.8V
 N=+2.5V
 M=+3.0V
 L=+3.3V
 H=+5.0V

Screening Level
 N = No Screening
 I = Industrial Std
 B = MIL-PRF-55310 , level B
 S = MIL-PRF-55310 , level S

Pin 1 Connection
 N=Not connected
 E=Enable/Disable

Frequency
 KHz/MHz

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Electrical Performance

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT			
Absolute Maximums	Maximum Supply Voltage	V_{CC}	-	-0.5	-	4.0	V			
	Storage Temperature	T_{STG}	-	-55	-	125	°C			
	Frequency Range (See Note 1)	f_0	-	1.0	-	160	MHz			
	Frequency Stability (See Note 2 and Ordering Information)	$\Delta f/f_0$	-	-	-	50	± ppm			
	Aging	$\Delta f/f_0$	-	-	-	3	± ppm/yr			
	Operating Temperature Commercial Industrial	T_A	-	-10 -40	25	70 85	°C			
Electrical and Waveform Parameters	Supply Voltage	V_{CC}	± 10 %	1.62 2.25 2.52 2.97	1.8 2.5 2.8 3.3	1.98 2.75 3.08 3.63	V			
	Supply Current	I_{CC}					mA			
	1.8V							-	-	30
	3.3V							-	-	40
	5V	-	-	50						
	Output Load	C_L				15	pF			
	Output Voltage Levels	V_{OH} V_{OL}	CMOS Load	90% V_{CC}	-	-	-	V		
	Logic '1' Level		CMOS Load	-	-	10% V_{CC}				
	Output Current	I_{OH} I_{OL}	$V_{OH} = 90\%V_{CC}$ (1.8V, 2.5/2.8V, 3.3V)	-	-	-2, -4, -8	mA			
	Logic '1' Level		$V_{OL} = 10\%V_{CC}$ (1.8V, 2.5/2.8V, 3.3V)	-	-	+2, +4, +8				
	Logic '0' Level									
	Output Duty Cycle	SYM	@ 50% Level	45	-	55	%			
	Rise and Fall Time	T_{R} , T_{F}	@ 10% - 90% Levels, $C_L = 15$ pF			10	ns			
	Start Up Time	T_S	Application of V_{CC}	-	-	10	ms			
	Enable Function	V_{IH} V_{IL}	Pin 1 Logic '1', Output Enabled	0.7* V_{CC}	-	-	V			
	Enable Input Voltage		Pin 1 Logic '0', Output Disabled	-	-	0.3* V_{CC}				
	Disable Input Voltage									
Enable Time	T_{PLZ}	Pin 1 Logic '1'	-	-	10	ms				
Standby Current	I_{ST}	Pin 1 Logic '0', Output Disabled	-	-	10	uA				
Period Jitter, Pk-Pk	-	-	-	-	100	ps				
Period Jitter, RMS	-	-	-	-	25					
Phase Jitter, RMS	-	Bandwidth 12 kHz - 20 MHz	-	< 2	-					

Note: 32.768KHz available